

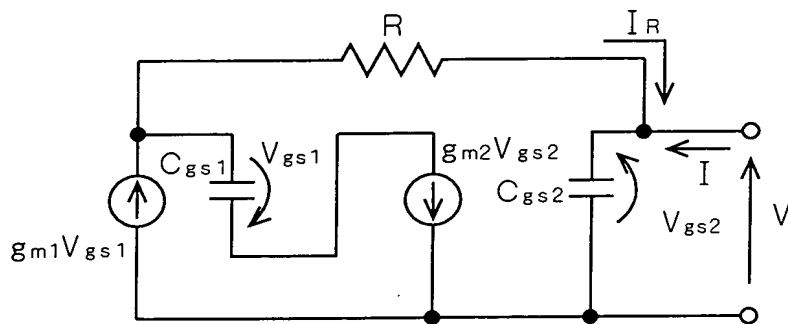
$$F / G. \quad 2$$


FIG. 4

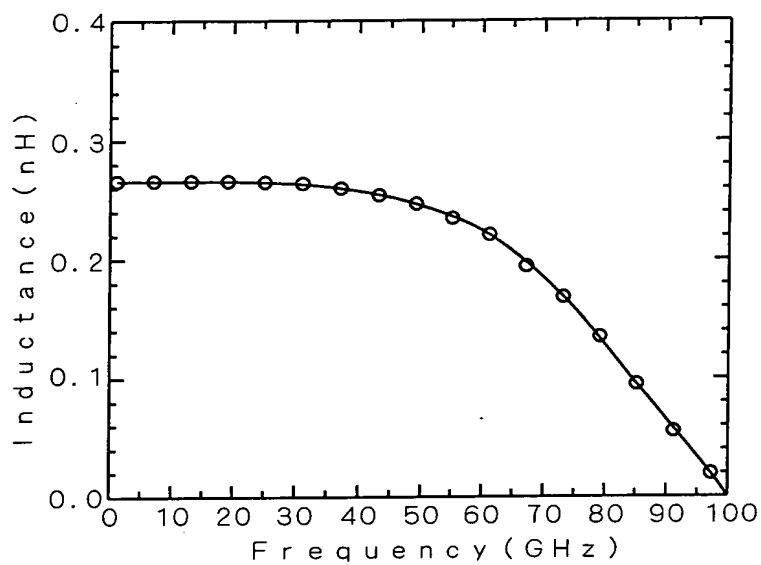


FIG. 5

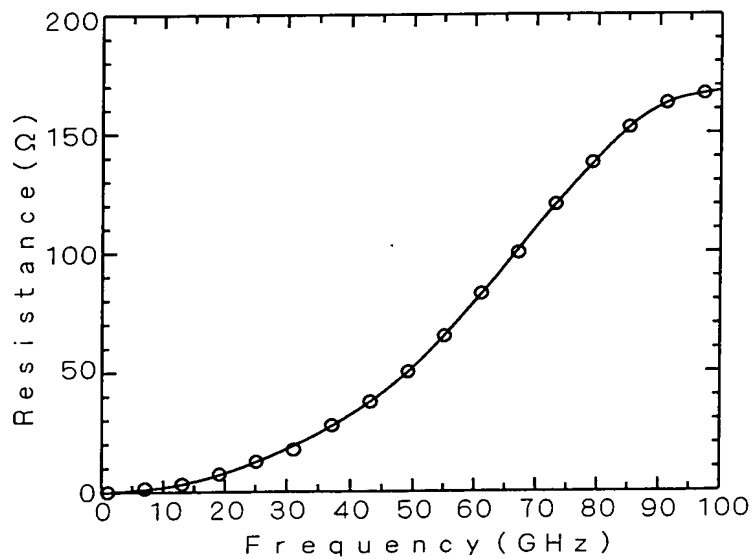


FIG. 6

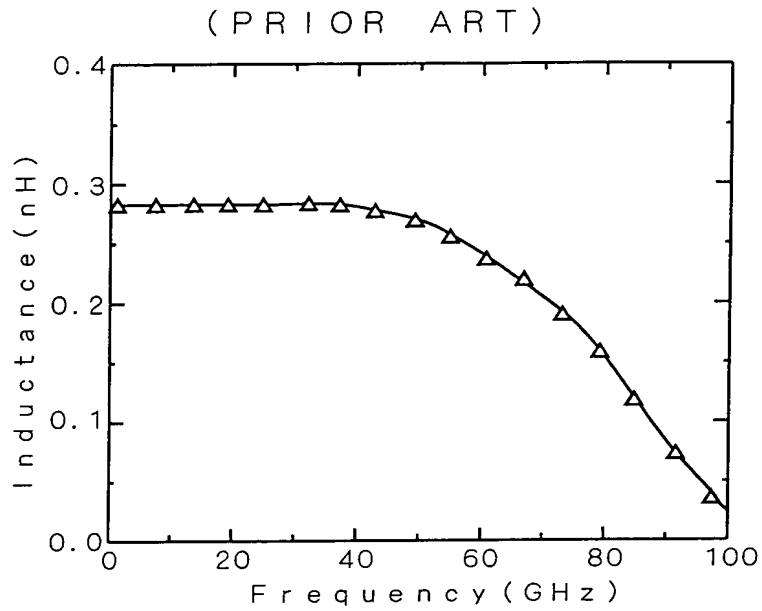


FIG. 7

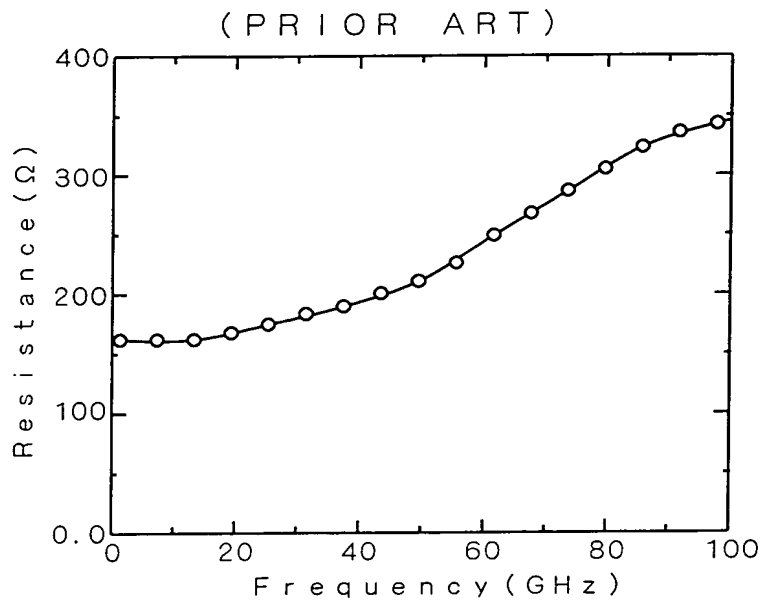
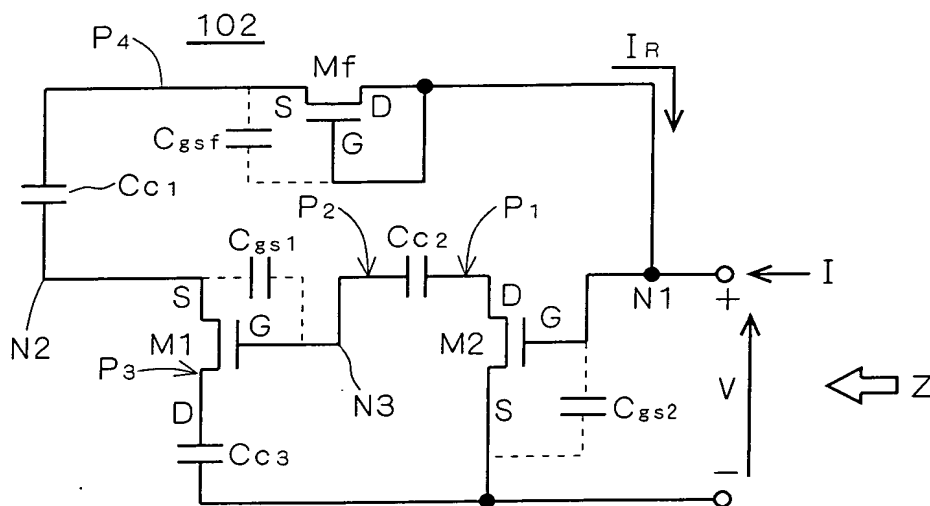


FIG. 8



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The diagram shows a differential amplifier circuit with two NMOS transistors, M1 and M2, whose sources are connected to ground. The gates of M1 and M2 are connected to a common gate node N3. A resistor R is connected between the gates of M1 and M2. The drain of M1 is connected to a supply voltage V through a load capacitor Cc1 and a load resistor R. The drain of M2 is connected to V through a load capacitor Cc2 and a load resistor R. The gates of M1 and M2 are biased by a common-mode feedback circuit consisting of a PMOS transistor M3 and a current source I. The gates of M1 and M2 are connected to the gates of M3 and M4, which are biased by a common-mode feedback circuit consisting of a PMOS transistor M3 and a current source I. The gates of M1 and M2 are connected to the gates of M3 and M4, which are biased by a common-mode feedback circuit consisting of a PMOS transistor M3 and a current source I. The gates of M1 and M2 are connected to the gates of M3 and M4, which are biased by a common-mode feedback circuit consisting of a PMOS transistor M3 and a current source I.

FIG. 10

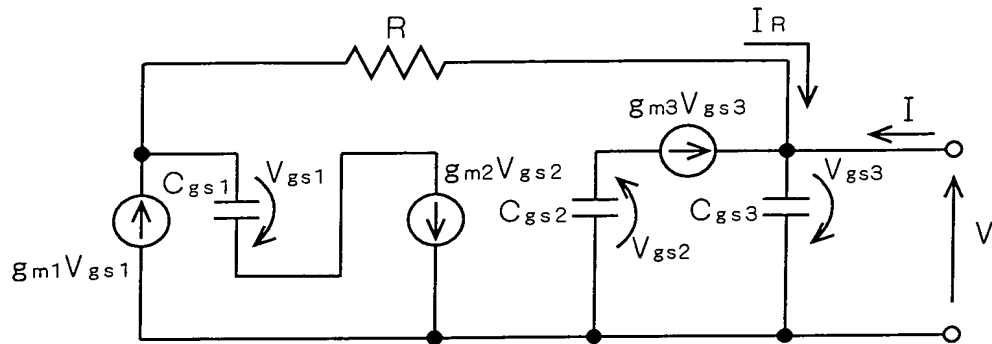


FIG. 11

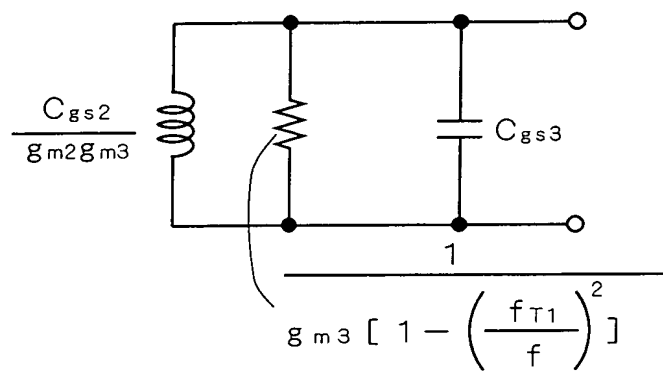


FIG. 12

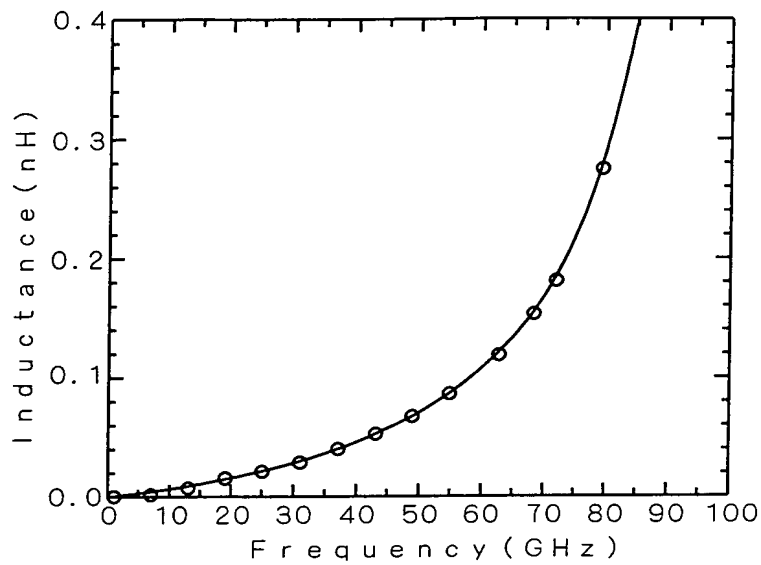


FIG. 13

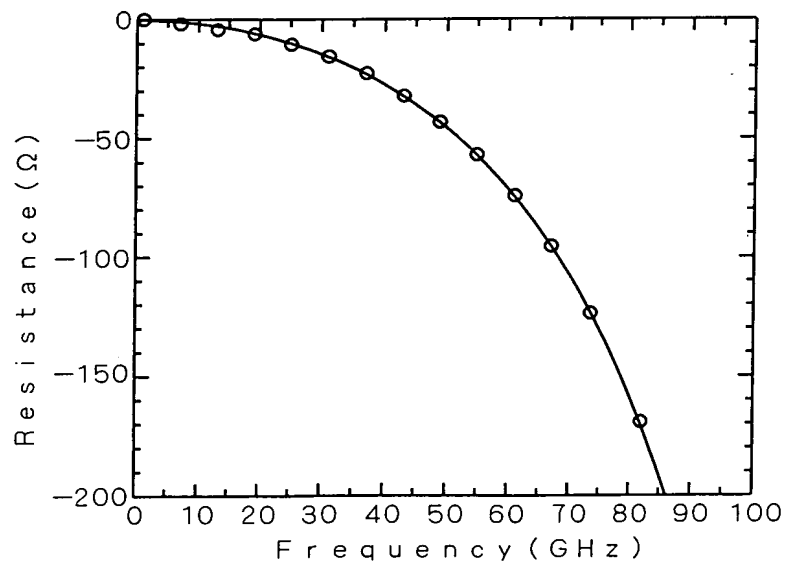
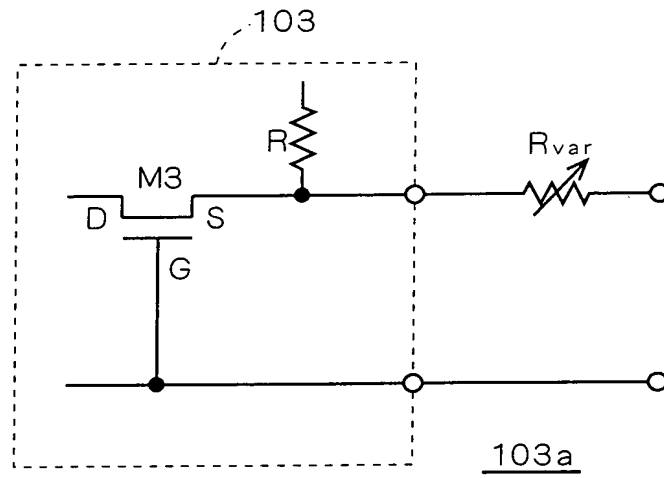


FIG. 14



REF ID: A65996

FIG. 16

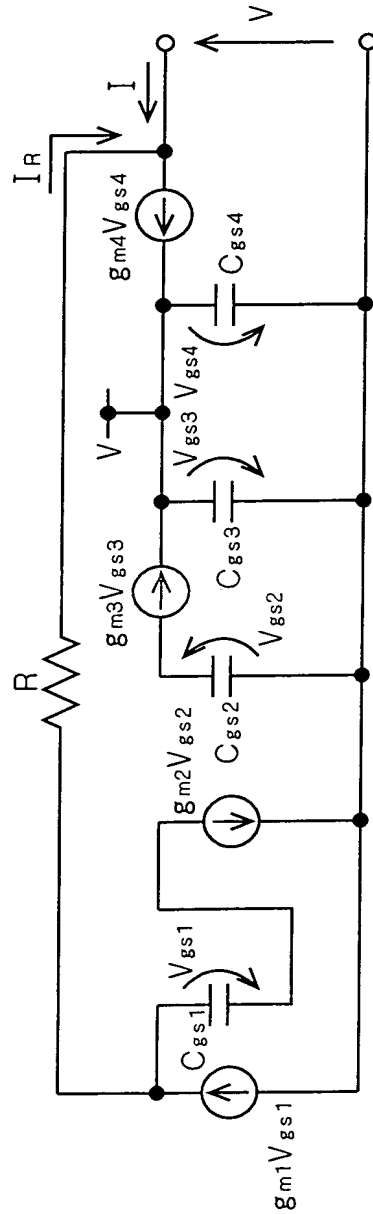


FIG. 17

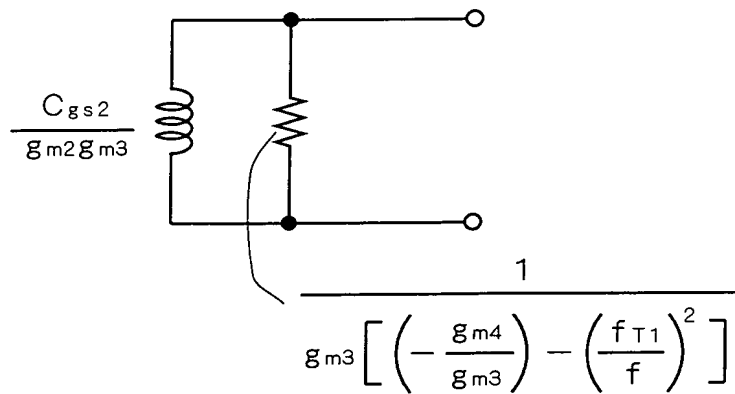


FIG. 18

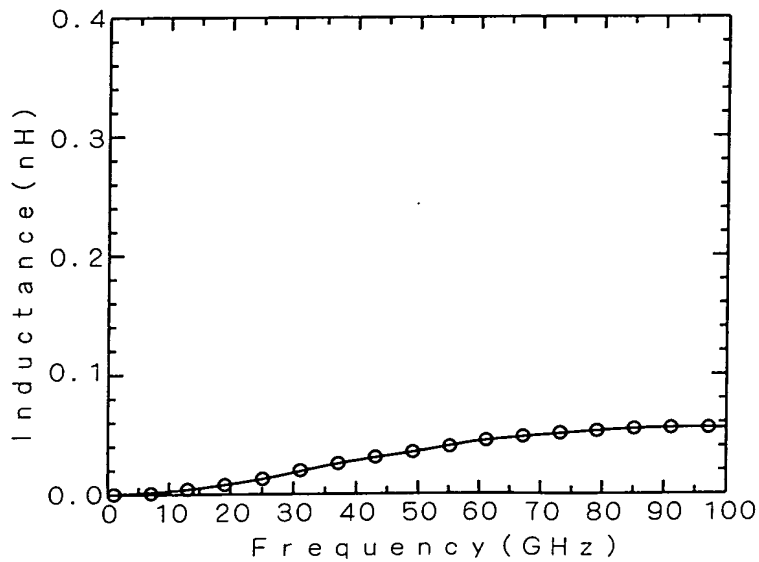


FIG. 19

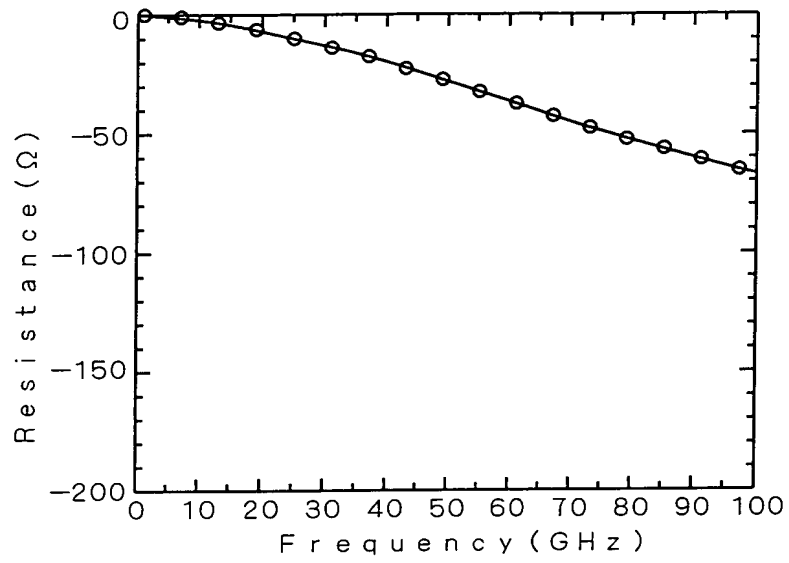


FIG. 20

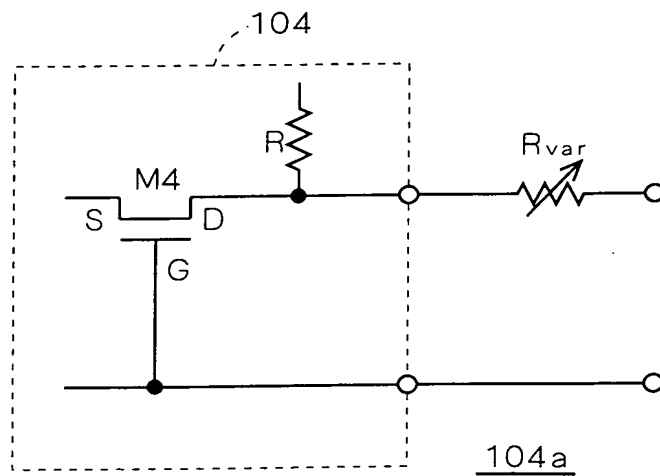


FIG. 21

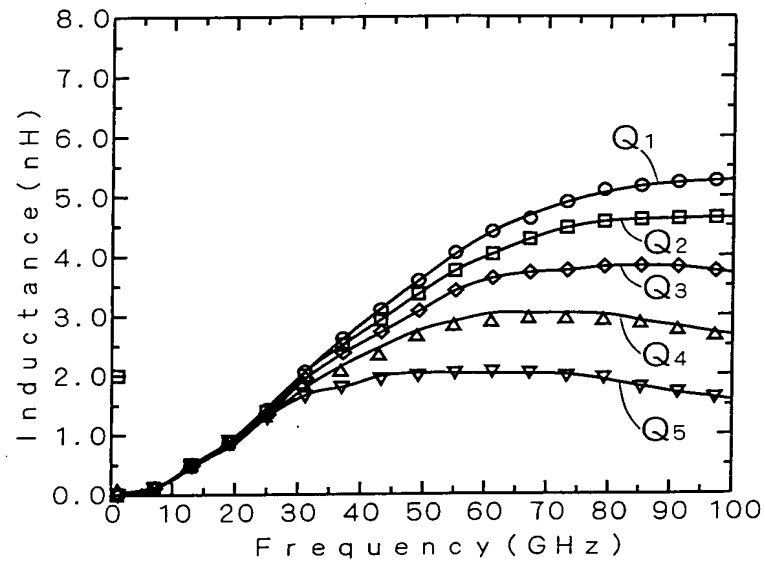


FIG. 22

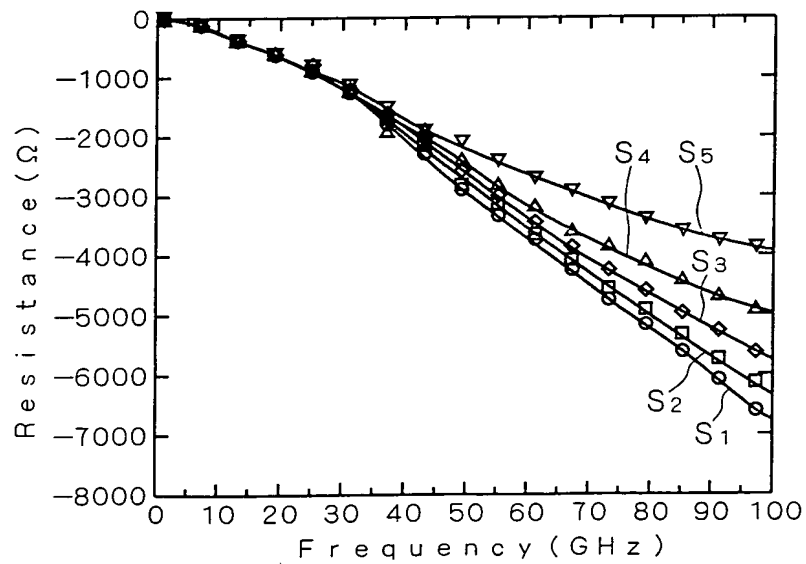


FIG. 23

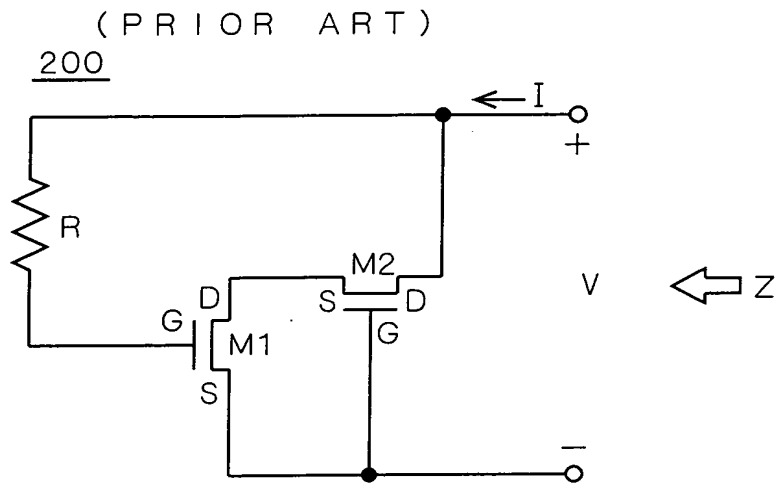


FIG. 24

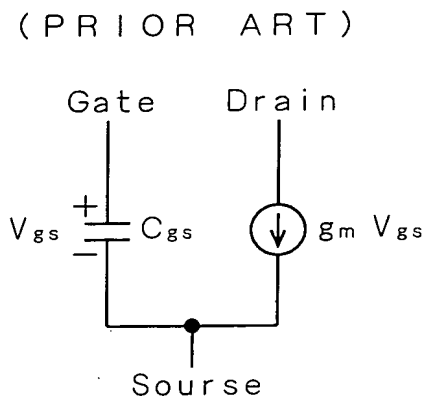


FIG. 25

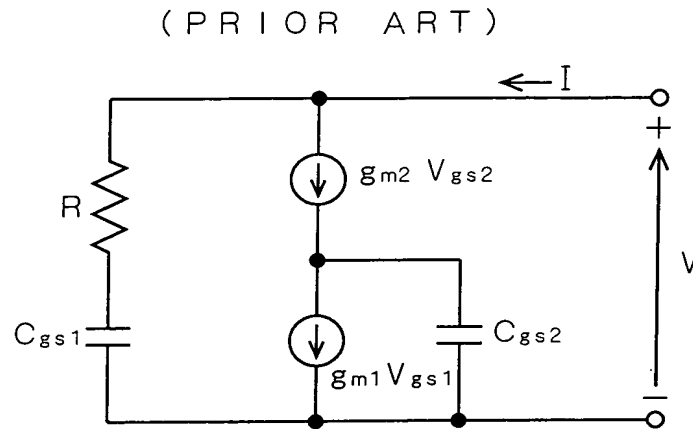


FIG. 26

